AMENDMENTS TO THE CLAIMS

Listing of the claims

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

1. (Currently Amended) A data processor comprising:

a receiving unit for receiving a series of data including a predetermined mark for detecting synchronization and generating parallel data from the series of data; and

a plurality of detecting units being provided at each bit position of the parallel data, ~~and for detecting said predetermined mark for detecting synchronization from the parallel data~~ the detecting units being adapted to detect whether strings of bits continuing from each bit position as a starting point are the predetermined mark; and

wherein any one of the detecting units detects the predetermined mark.

2. (Currently Amended) A data processor according to claim 1, wherein said plurality of detecting units detect the predetermined mark ~~marks~~ for detecting synchronization in a predetermined bit width among the series of data in parallel condition.

3. (Currently Amended) A data processor according to claim 1, further comprising a generation timing selecting unit for selecting generation timing of a window for detecting the predetermined mark ~~marks~~ based on the predetermined mark ~~marks~~ for detecting synchronization.

4. (Currently Amended) A data processor according to claim 1, further comprising a data demodulating unit for demodulating the series of data between the predetermined mark ~~marks~~ for detecting synchronization based on the predetermined mark ~~marks~~ for detecting synchronization.

5. (Currently Amended) A data processor according to claim 1, further comprising a detection line memory unit for storing a detection line based on the predetermined mark ~~marks~~ for detecting synchronization.

6. (Currently Amended) A data processor according to claim 1, further comprising a data selecting unit for selecting data based on the predetermined mark ~~marks~~ for detecting synchronization.

7. (Currently Amended) A data processor according to claim 1, further comprising a data counting unit for counting the series of data between the predetermined mark ~~marks~~ for detecting synchronization based on the predetermined mark ~~marks~~ for detecting synchronization.

8. (Canceled).

9. (Previously Presented) A data processor according to claim 1, wherein said receiving unit is provided with a shift register to input the plurality of parallel data connected with the detecting units in the same number as the number of parallel data.

10. (Currently Amended) A data processor for detecting a predetermined mark for detecting synchronization included in a series of data read from a memory medium in order to establish synchronization at a time of transferring the series of data to a controller unit from a read channel unit, comprising:

a receiving unit for receiving the series of data including the predetermined mark for detecting synchronization and generating parallel data from the series of data; and

a plurality of detecting units being provided at each bit position of the parallel data, ~~and for detecting said predetermined mark for detecting synchronization from the parallel data~~ the detecting units being adapted to detect whether strings of bits continuing from each bit position as a starting point are the predetermined mark; and

wherein any one of the detecting units detects the predetermined mark.

11. (Currently Amended) A data processing method comprising the following steps of:

receiving a series of data including a predetermined mark ~~marks~~ for detecting synchronization;

generating a ~~plurality of~~ parallel data from the series of data;

detecting the predetermined mark ~~marks~~ for detecting synchronization from ~~said plurality of parallel data~~ any one of strings of bits continuing from each bit position of the parallel data to establish synchronization of the series of data; and

demodulating the series of data based on the predetermined mark ~~marks~~ for detecting synchronization detected from one of the bit strings ~~included in the series of data~~.

12. (Currently Amended) A data processing method according to claim 11, wherein the predetermined mark ~~marks~~ for detecting synchronization are detected in predetermined bit widths of the series of data in parallel condition.

13. (Currently Amended) A data processing method according to claim 11, wherein generation timing of a window for detecting predetermined mark ~~marks~~ is selected based on the detected predetermined mark ~~marks~~ for detecting synchronization.

14. (Currently Amended) A data processing method according to claim 11, wherein a detection line is stored based on the detected predetermined mark ~~marks~~ for detecting synchronization.

15. (Currently Amended) A data processing method according to claim 11, wherein data is selected based on the detected predetermined mark ~~marks~~ for detecting synchronization.

16. (Currently Amended) A data processing method according to claim 11, wherein data between the detected predetermined mark ~~marks~~ for detecting synchronization is counted up.

17. (Canceled)

18. (New) A data processor according to claim 1, wherein the plurality of detecting units are provided in equal number to the number of bits constituting the parallel data.

19. (New) A data processor according to claim 10, wherein the plurality of detecting units are provided in equal number to the number of bits constituting the parallel data.